

We claim:

1. A probe card configuration for testing a plurality of integrated circuits in parallel using a test system having electrical signal lines, the probe card configuration comprising:

a carrier board for receiving said electrical signal lines of said test system, said carrier board defining a plane;

contact-making needles for producing electrical connections with contact areas on the integrated circuits to be tested, said contact-making needles for connection with said electrical signal lines of said test system to produce signal paths between said test system and the integrated circuits to be tested; and

a plurality of active modules configured on said carrier board, each one of said plurality of said active modules being assigned to one of the integrated circuits to be tested in parallel, each one of said plurality of said active modules being inserted into ones of the signal paths that are between said test system and the respective assigned one of the integrated circuits to be tested, each one of said plurality of said active modules having a longest extent;

said longest extent of each one of said plurality of said active modules being configured non-parallel with said plane of said carrier board.

2. The probe card configuration according to claim 1, wherein said longest extent of each one of said plurality of said active modules is configured at right angles with respect to said plane of said carrier board.

3. The probe card configuration according to claim 1, in combination with the plurality of the integrated circuits, wherein:

the plurality of the integrated circuits are a plurality of fast semiconductor memory modules that are located on a wafer.

4. The probe card configuration according to claim 1, in combination with the plurality of the integrated circuits, wherein:

each one of the plurality of the integrated circuits has a longest extent; and

said longest extent of each one of said plurality of said active modules is greater than the longest extent of the assigned one of the integrated circuits to be tested.

5. A method for testing a plurality of integrated circuits on a wafer in parallel, which comprises:

providing the probe card configuration according to claim 1;

making contact between a first group of the integrated circuits to be tested on the wafer and said contact-making needles;

performing a test routine with the first group of the integrated circuits to be tested;

making contact between a second group of the integrated circuits to be tested on the wafer and said contact-making needles, the second group of the integrated circuits being located disjunct with respect to the first group of the integrated circuits;

performing a test routine with the second group of the integrated circuits to be tested;

configuring the integrated circuits to be tested on the wafer in a regular rectangular grid form having main directions at right angles to one another;

configuring the first group of the integrated circuits and the second group of the integrated circuits to extend along the main directions of the grid;

performing the step of making contact between the first group of the integrated circuits and said contact-making needles such that a given one of the integrated circuits is located between two of the integrated circuits of the first group in one of the main directions, and the given one of the integrated circuits is not tested in parallel with the first group of the integrated circuits; and

performing the step of making contact between the second group of the integrated circuits and said contact-making needles such that another given one of the integrated circuits is located between two of the integrated circuits of the second group in one of the main directions, and the other given one of the integrated circuits is not tested in parallel with the second group of the integrated circuits.

6. A method for testing a plurality of integrated circuits on a wafer in parallel, which comprises:

providing the probe card configuration according to claim 1;

making contact between a first group of the integrated circuits to be tested on the wafer and said contact-making needles;

performing a test routine with the first group of the integrated circuits to be tested;

making contact between a second group of the integrated circuits to be tested on the wafer and said contact-making needles, the second group of the integrated circuits being located disjunct with respect to the first group of the integrated circuits;

performing a test routine with the second group of the integrated circuits to be tested;

configuring the integrated circuits to be tested on the wafer in a regular rectangular grid form having diagonals; and

configuring the first group of the integrated circuits and the second group of the integrated circuits to extend along the diagonals of the grid.